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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/830,006	04/23/2004	Zoran Krivokapic	H1108C	7644

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/830,006	KRIVOKAPIC ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-18* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *(3 pages)*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 04/23/2004 is acceptable.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 5, 2-4, 6-10, 16, 11-15, and 17 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of U.S. Patent No. 6,762,483. Although the conflicting claims are not identical, they are not patentably distinct from each other. Claims 1, 5, 2-4, 6-10, 16, 11-15, and 17 of the present invention is a similar version of the claimed invention in claims 1-14 of the above-identified U.S. Patents with similar intended scope.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1, 3, 5, 7-11, 13-14, and 17** are rejected under 35 U.S.C. 102(e) as being anticipated by Adkisson et al. U.S. Patent 6,472,258.

Adkisson discloses in Figures 1-5 and respective portions of the specification a MOSFET device and a method for forming thereof as claimed.

Referring to **claim 1**, Adkisson discloses a MOSFET device comprising:

a source and a drain (defined by a mask labeled generally as "active area mask", Figs. 3 and paragraph bridging columns 3 and 4) formed on an insulating layer ("Buried Oxide");

a fin structure (defined generally by the horizontal section that together with the two vertical sections of Fig. 3A forms an "H", in Fig. 3, the fin structure is simply labeled as "Si") formed on the insulating layer between the source and the drain, the fin structure including a first region formed in a channel area of the fin structure (paragraph bridging columns 3 and 4);

a protective layer (16, Figs. 1 through 3) formed over at least the first region of the fin structure, the protective layer being wider than the first region (best seen in Fig. 3); and

a gate ("gate polysilicon") formed on the insulating layer around at least a portion of the fin structure.

Referring to independent **claim 10** and using the same reference characters and citations as detailed above where applicable, Adkisson discloses a method for forming a MOSFET device comprising:

forming a source, a drain, and a fin structure on an insulating layer, portions of the fin structure acting as a channel for the MOSFET;

forming a protective layer above the fin structure;

trimming the fin structure without significantly trimming the protective layer (column 3, lines 20-29); and

depositing a polysilicon layer to act as a gate area for the MOSFET.

Referring to independent **claim 17** and using the same reference characters and citations as detailed above where applicable, Adkisson discloses a device comprising:

a source and drain;

a fin structure formed between the source and the drain, the fin structure including a first region formed in a channel area of the fin structure and a second and third protective region (16, "pad nitride" and note that the protective region is disclosed as comprising pad nitride and pad oxide – column 3, lines 10-15 – hence the protective region 16 comprises a second protective region and a third protective region) formed adjacent the source and drain, respectively, wherein the first region is narrower than the second and third protective regions; and

a gate formed around at least a portion of the fin structure.

Referring to **claim 3**, as noted above, Adkisson discloses that the protective layer includes an oxide layer (pad oxide) and a nitride layer (pad nitride) formed over the oxide layer.

Referring to **claim 5**, Adkisson further discloses a dielectric layer ("gate oxide", Fig. 3) formed around at least a channel portion of the fin structure.

Referring to **claim 7**, as noted above, Adkisson discloses that the gate comprises polysilicon.

Referring to **claim 8**, although Adkisson does not call the MOSFET device a FinFET, Adkisson's MOSFET could be called a FinFET because it is a FET having a body or channel region including a fin structure.

Referring to **claim 9**, the gate of the Adkisson's MOSFET is formed to include small gate lengths (BACKGROUND OF THE INVENTION section, and "small" is interpreted broadly).

Referring to **claim 11**, Adkisson further discloses that the fin structure is trimmed by exposing the fin structure to NH4OH (column 3, lines 30-35).

Referring to **claim 13**, Adkisson further discloses depositing a tetraethylorthosilicate (TEOS) layer over the MOSFET device before trimming the fin structure (paragraph bridging columns 3 and 4: "...TEOS is deposited and the active area patterned as shown in FIG. 3A...", and note that the active area including the fin structure).

Referring to **claim 14**, Adkisson further discloses etching away the TEOS layer over the fin structure before trimming the fin structure (column 4, lines 25-28: "the disposable active area hard mask is applied and patterned and etching to the BOX is performed as before", and note that the disposable active area hard mask is the TEOS and that "over" in "over the fin structure" is interpreted broadly).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 2 and 16** are rejected under 35 U.S.C. §103(a) as being unpatentable over Adkisson in view of Fried et al. U.S. Patent 6,750,487 or Lee et al. U.S. Patent 6,768,158.

Adkisson discloses a MOSFET device and a method for forming thereof as claimed and as detailed above including the step of trimming the fin structure but fails to discloses that the first region of the fin structure has, or trimming the fin structure to, a width of about 3 nm to 6 nm. Fried, also in disclosing a MOSFET having a fin structure, teaches that the fin thickness should (only) be greater that 2.5 nm to avoid degraded mobility due to quantum confinement issues (column 3, lines 56-60); and Lee, also in disclosing a MOSFET having a fin structure, teaches that fin thickness is normally in the range of 3 nm to 50 nm (column 5, lines 5-8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the fin structure of Adkisson's MOSFET device with a width of about 3 nm to 6 nm. One would have been motivated to make such a modification in view of the teachings in Fried that fin thickness should only be greater that 2.5 nm, hence an ordinary skill in the art could easily arrive at about 3 nm to 6 nm, to avoid degraded mobility due to quantum confinement issues; or one would have been motivated to make such a modification in view of the teachings in Lee that fin thickness is normally in the range of 3 nm to 50 nm, hence an ordinary skill in the art could easily arrive at about 3 nm to 6 nm.

6. **Claims 4, 6, 12, and 18** are rejected under 35 U.S.C. §103(a) as being unpatentable over Adkisson.

Referring to **claims 4 and 12**, Adkisson discloses a MOSFET device and a method for forming thereof as claimed and as detailed above including the oxide layer and the nitride layer,

and further discloses that the oxide layer is about 3-10 nm and the nitride layer is about 100 nm (column 3, lines 12-15) instead of the claimed 15 nm and 50 nm – 75 nm, respectively. However, since the criticality of the various sizes has not been established, it would seem that one of ordinary skill in the art at the time the invention was made could freely and easily choose from the different various sizes.

Referring to **claim 6**, Adkisson discloses a MOSFET device as claimed and as detailed above including the dielectric layer ("gate oxide" or "gate dielectric"), and further discloses that the dielectric layer is about 1-2 nm (column 3, lines 36-39) instead of the claimed about 0.6 nm to 1.2 nm. However, since the criticality of the various thickness has not been established, it would seem that one of ordinary skill in the art at the time the invention was made could freely and easily choose from the different various thickness.

Referring to **claim 18**, Adkisson discloses a MOSFET device as claimed and as detailed above including the first region, the second and third regions, the first region is thinner that the second and third regions, but fails to discloses that the first region is approximately 4 to 12 nm thinner than the second and third regions. However, the limitation "approximately 4 to 12 nm" in "the first region is approximately 4 to 12 nm thinner than the second and third regions" is deemed to be obvious because, similarly as explained thus far, the criticality of the dimension has not been established, especially in the instant case the limitation has not even been mentioned in the detailed specification and the original disclosure.

Allowable Subject Matter

7. **Claim 15** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a method for forming a MOSFET having all limitations as recited in claims 10, 13, and 15, and characterized in the limitations of claim 15.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
November 02, 2004